VDMOS - Subcircuit - Modeling and Model Parameter Extraction [1]

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Abstract - This paper deals with DC modeling of integrated VDMOS transistors using subcircuit models. The advantage of a subcircuit model is that it can be used with all versions of the SPICE simulator without any problems. In the following article, some models are described and model parameter procedures are explained. The models have been tested with SPICE3d2 and PSPICE 5.0.

1. Introduction

For a variety of reasons the VDMOS transistor behaviour differs from the usual MOSFET behaviour. For high gate voltages the input characteristic $I_D = f(V_G)$ deviates from the ideal square law .This is often called the VDMOS quasi saturation /25/. The equation for the pinch off range[2] is

$$I_D = K_P * (V_{GS} - V_{TH})^2 \qquad (1)$$

This is not valid at high gate voltages because the drain current calculated by eqn. 0 at such operating points is too high. The SPICE3 - MOS - models Level 1, 2 and 3 are not able to simulate this VDMOS behaviour. As may be seen from eqn. 1, in principle three different ways are possible to solve the problem:

- Reduction of transconductance K_P : This is possible using UCRIT and UEXP for Level 2 or VMAX and THETA for Level 3 respectively. However this way gives no sufficient agreement between simulated and measured lines in the whole characteristic range [3].
- Reduction or compliance respectively of the drain current, realized by a current dependent drain resistance /27/ or by a cascaded JFET /28, 29/ [4].

[1] Article for the HP - IC-CAP - Usermeeting Den Haag Sept.1995, file: um67e.doc, 13.9.95

[2] Note: W / L = 1

[3] Changing a model parmeter (K_P, V_{TH}) depending on the operating point is not possible in SPICE3.

[4] Using a JFET is in accordance to real VDMOS structure (Fig. 2).

- Reduction of the effective gate voltage, using a transformation by a voltage controlled voltage source (VCVS) or a current dependent source resistance /26/.

This paper is mainly concerned with the JFET subcircuit and the VCVS subcircuit version.

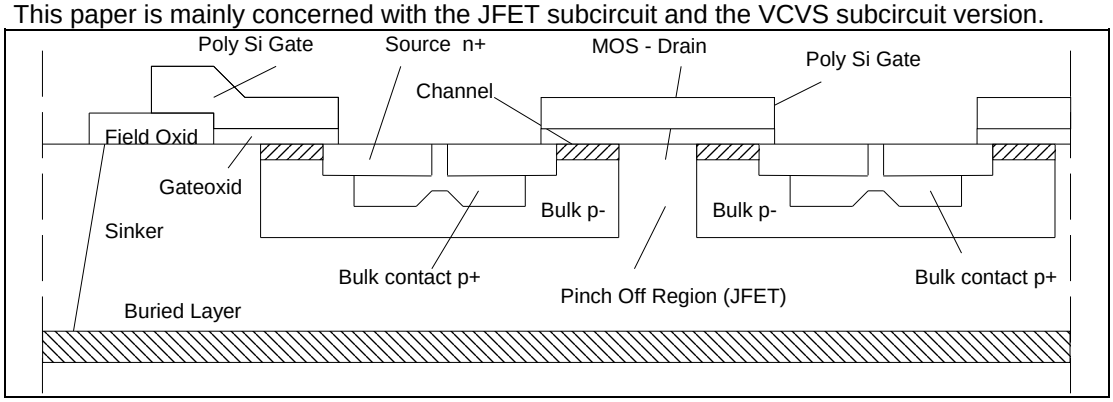

Fig. 2: Cross section of an integrated VDMOS transistor

2. Subcircuit Model using MOS and JFET

2.1. Subcircuit Function

As can be seen from Fig. 2, one can derive an equivalent circuit according to Fig. 3A from the real VDMOS structure. The p - bulk acts as the JFET gate. It is always shorted to the source for a VDMOS. The epitaxial layer below the gate acts as the MOS drain and as the JFET source at the same time. The "nick area" underneath this range, created by the neighbouring p - wells, acts as the JFET channel. It is pinched off by the p -well / epitaxy depletion layer.

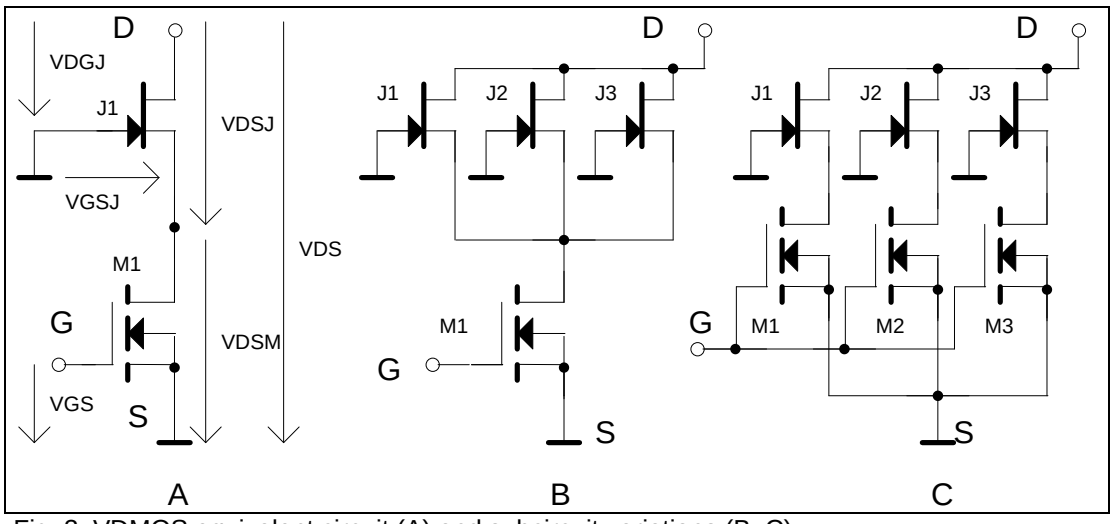

Fig. 3: VDMOS equivalent circuit (A) and subcircuit variations (B, C)

From Fig. 3A we have the following main equations[5]:

$$I_{DM} = I_{DJ} \quad (4)$$

$$V_{DSM} = -V_{GSJ} \quad (5)$$

$$V_{DS} = V_{DGJ} \quad (6)$$

$$V_{DS} = V_{DSM} + V_{DSJ} \quad (7)$$

Considering the function of the MOS - JFET - subcircuit, we have to decide two different cases:

Case 1: Drain Current Compliance

[5] Note the indizes: M = MOS, J = JFET.

This case occurs if the JFET current I_{DSS} and the maximum MOS current are in the same order. The operating point of the MOS - JFET subcircuit is given by superposition of the MOS output and the JFET transfer characteristic (Fig. 8). For a given gate voltage V_{G1} the MOS drives a drain current I_D into the JFET. The MOS drain source voltage will adjust now to the point P1, at which both the MOS and the JFET drain currents are equal. If the MOS gate voltage increases now to V_{G2} , the MOS drain current increases also. To conduct this current through the JFET, a decrease of the JFET gate source voltage is necessary. The inner drain potential (V_{DSM}) decreases and a new operating point P2 is found. As can be seen in Fig. 8, the drain current variation of I_D in curve B is lower than the variation of I_{DM} without JFET in curve A. That means the JFET acts as a drain current compliance.

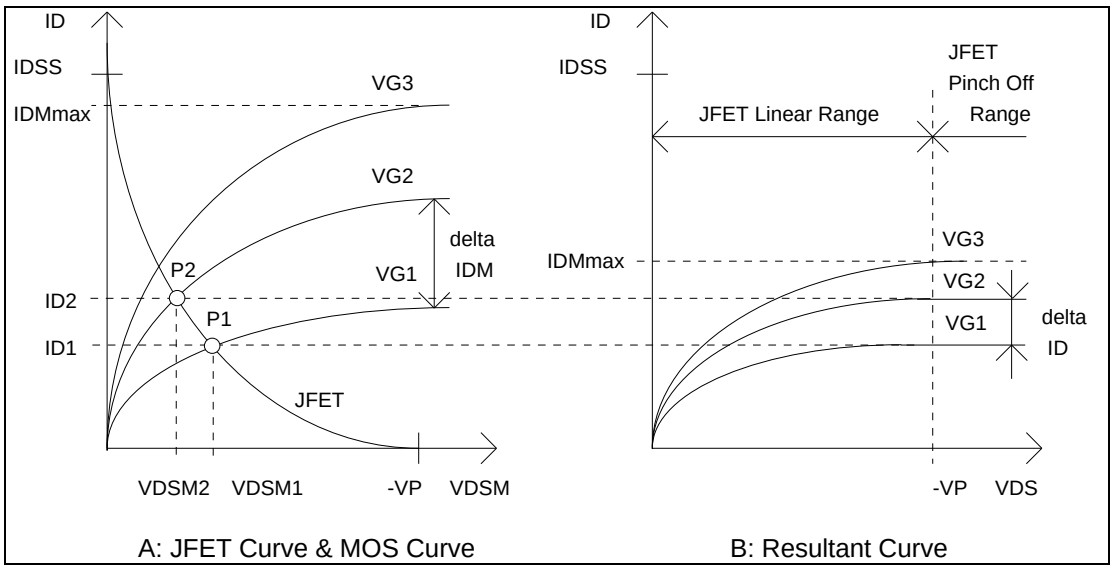

Fig. 8: Superposition of JFET transfer and MOS output characteristic (A) and the resultant output characteristic (B) for case 1: $I_{DSS} \approx I_{DSMmax}$ [6]

Case 2: Drain Voltage Compliance

This case occurs if the JFET transconductance model parameter is set to a very high value, e.g. BETA = 100 * KP /28/. This means that the maximum JFET current I_{DSS} is much higher than the maximum MOS drain current. The JFET now always works at gate voltages near the pinch off voltage V_P . We can observe a sharp break in resultant output characteristic for the

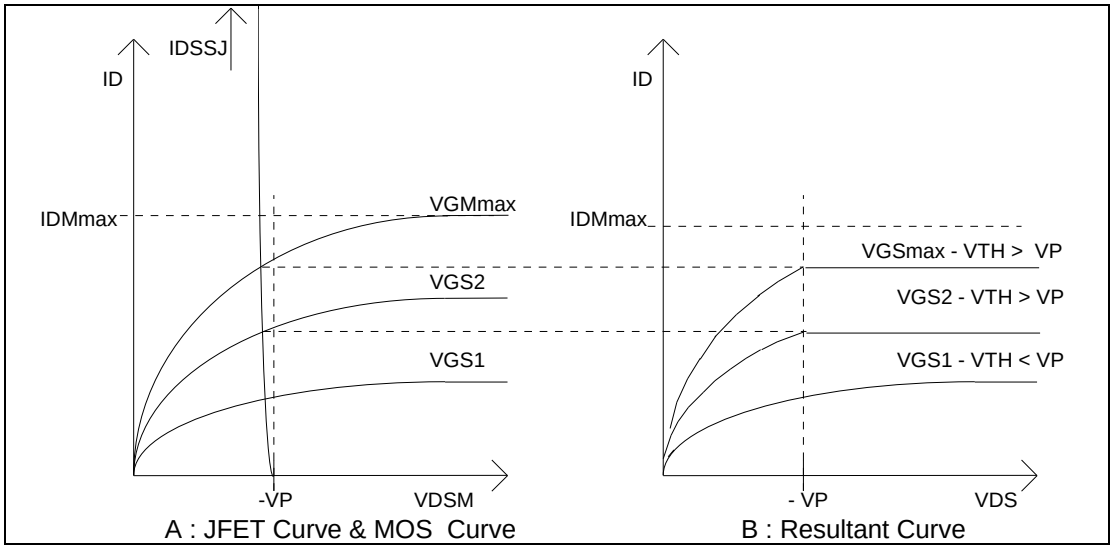

Fig. 9: JFET transfer and MOS output characteristic (A) and the resultant output characteristic (B) for case 2 : $I_{DSS} >> I_{DM\ max}$

[6] Note: x - axis for A is V_{DSM} , x - axis for B is V_{DS}

curves, which comply with the condition V_{GS} - V_{TH} > V_P . The reason for this is the limitation of the MOS drain source voltage V_{DSM} to the value of V_P . According to eqn. 5 the maximum value of V_{DSM} is given by V_P . So the MOS is not able to pass over into the pinch off range. It is forced to remain in the linear range. For a given gate voltage the drain current in the linear range depends on V_{DS} only. Thus the voltage compliance results in a current compliance again, but the value is different from case 1.

Continuing the JFET - MOS subcircuit analysis we have to decide which of the two devices are in the linear or in the pinch off range. That is simple for the JFET if we define the pinch off condition by

$$V_{DGp} = -V_P \tag{10}$$

instead of the usual equation

$$V_{DSp} = V_{GS} - V_P \tag{11}$$

Because of eqn. 6 we can draw a vertical line at V_{DS} = - V_P in the resultant output characteristic, divide off the linear and the pinch off range (Fig. 8B).

Considering the MOS now, the linear range is defined as

$$V_{DSM} < V_{GS} - V_{TH} \tag{12}$$

We can determine V_{DSM} by calculating the JFET gate source voltage. Using the square law for the pinch off range V_{DS} - V_P

$$I_D = BETA * (V_{GSJ} - V_P)^2 \tag{13}$$

we can write

$$V_{GSJ} = \sqrt{\frac{I_D}{BETA}} + V_P = -V_{DSM} \tag{14}$$

As may be seen, I_{DSM} decreases if I_D and sqrt(ID/BETA) increases[7]. If V_{GS} is sufficient high, the MOS acts in the linear range. By rearranging eqn. 0 and 0 one can define this condition as:

$$V_{GS} > \sqrt{\frac{I_D}{BETA}} + V_P + V_{TH} \tag{15}$$

Summarising the resultant characteristic of the MOS - JFET subcircuit we can say:

- The MOS operating point depends on the gate voltage. For sufficient high values, it works in the linear range.
- The JFET turns from linear to pinch off range at V_{DS} = - V_P .

2.2. Subcircuit Variations

Using the simple principle circuit according to Fig. 0A it was not possible to accomplish a good agreement for the VDMOS transistors under investigation . That is why we used the modified circuit Fig. 0C with additional branches. The three MOS devices all have the same threshold voltage V_{TH} and each one a third of the transconductance K_P . For the JFET devices we vary either both BETA and V_P (for case 1) or only V_P (for case 2) in such a manner that they will effect the resultant characteristic at different V_{DS} values. That gives an improved modeling of the curvature in the linear range.
Finally we used negative values for the JFET parameter LAMBDA for modeling the typical decrease of the VDMOS output characteristic at high gate and drain voltages.

[7] Note: U_P is negativ.

2.3. Model Parameter Determination

2.3.1. MOS - Parameter V_{TH} , K_P and R_S

Determining the threshold voltage and the transconductance we used the following well known method. Using a plot SQRT I_D = f (V_{GS}) the slope in the linear zone gives K_P and the x - axis intercept gives V_{TH} (condition: the device is in the pinch off range).

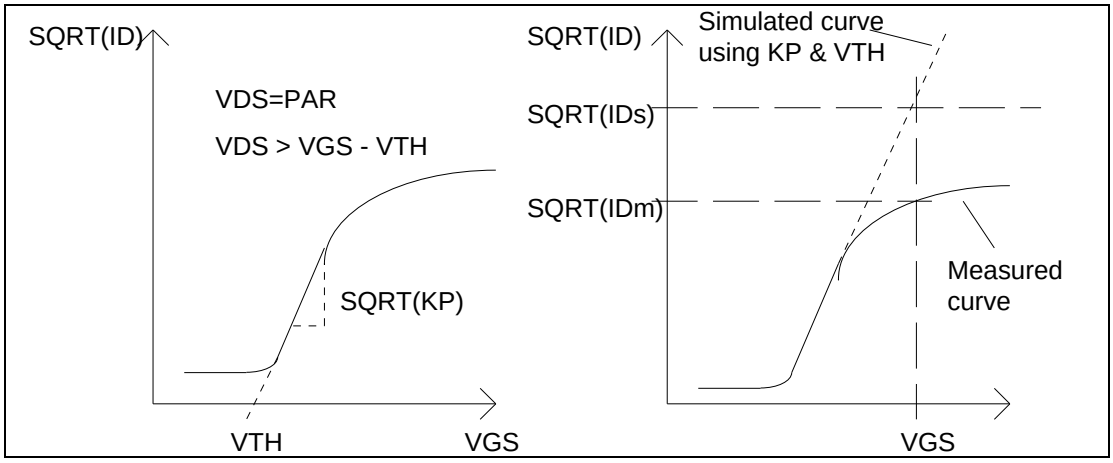

Fig. 16: Determination of MOS parameter V_{TH} , K_P and R_S

We can determine the source resistance using the transfer characteristic also. Assuming R_S as the only reason for deviations between the simulated line (using K_P and V_{TH} , determined in advance) and the measured line, we are able to calculate R_S [8].
For the simulated line (index = s) and the measured line (index = m) respectively we have:

$$\sqrt{I_{Ds}} = K_P * \left[V_{GS} - V_{TH}\right] \tag{17}$$

$$\sqrt{I_{Dm}} = K_P * \left[V_{GS} - V_{TH} - I_{Dm} * R_S\right] \tag{18}$$

Using the ratio of eqn. 0 and 0 the source resistance can be calculated as:

$$R_S = \frac{V_{GS} - V_{TH}}{I_{Dm}} * \left[1 - \sqrt{\frac{I_{Ds}}{I_{Dm}}}\right] \tag{19}$$

As we have found this equation results in a R_S value that increases with increasing gate voltage. The reason is the incorrect assumption we made. In reality R_S is **not** the only reason for the deviations between measured and simulated line. That is why we should determine R_S in the low gate voltage range.

2.3.2. JFET - Parameter V_P and BETA

Determining the JFET parameter, we have to decide the two cases again:

Case 1: Drain Current Compliance

In this case the parameter determination is complicated, because we are able to measure only the drain current, but not the appropriate JFET gate voltage. Thus it is necessary to derive an equation between the JFET gate voltage V_{GSJ} and the external MOS gate voltage V_{GS} . To solve the problem we consider the range V_{DS} - V_P, then the JFET is in the pinch off and the MOS is in the linear range.
Using two curves of the resultant output characteristic and the operating point values V_{GS1} , I_{D1} and V_{GS2} , I_{D2} and taking into account eqn. 14 we can write the difference JFET gate voltage :

[8] Note: To eliminate the drain voltage effect (LAMBDA) make this measurement under condition V_{DS} = V_{GS} - V_{TH} , or nearly V_{DS} = V_{GS} (drain and gate shorted).

$$\Delta V_{GSJ} = \frac{1}{\sqrt{BETA}} * \left[\sqrt{I_{D2}} - \sqrt{I_{D1}} \right] \quad (20)$$

The MOS is described in the linear range by

$$I_D = K_P \left[(V_{GS} - V_{TH}) V_{DSM} - \frac{1}{2} {V_{DSM}}^2 \right] \quad (21)$$

or for low drain source voltage values approximately:

$$I_D = K_P \left[(V_{GS} - V_{TH}) V_{DSM} \right] \quad (22)$$

Using two operating points again and rearranging eqn. 0 gives:

$$\Delta V_{DSM} = \frac{1}{K_P} \left[\frac{I_{D2}}{V_{GS2} - V_{TH}} - \frac{I_{D1}}{V_{GS1} - V_{TH}} \right] \quad (23)$$

Combining eqn. 20 and 23 we get a relationship for BETA:

$$BETA = \frac{{K_P}^2 * \left[\sqrt{I_{D2}} - \sqrt{I_{D1}} \right]^2}{\left[\frac{I_{D2}}{V_{GS2} - V_{TH}} - \frac{I_{D1}}{V_{GS1} - V_{TH}} \right]^2} \quad (24)$$

For the application of this relationship it is necessary to choose two measured curves, at which the JFET already shows a clear effect, i.e. at high gate voltages. Using this BETA one can determine the appropriate V_P value by curve fitting to the maximum current value in the pinch off range. Generally at this stage the agreement of measured and simulated lines in the linear range will still be unsatisfactory. Thus it will be necessary again to use a model with several branches according to Fig. 0B, C. For that reason we have to vary the pinch off voltage V_P and to divide the transconductance BETA for the three JFET devices, satisfying the condition that the whole maximum current

$$\sum_1^n I_{DSS} = K_{Pn} * {V_{Pn}}^2 \quad (1)$$

is held constant. The use of the case 1 parameter determination is more complicated than in case 2, but it may give a better agreement between measured and simulated lines without sharp breaks in the characteristics.

Case 2: Drain Voltage Compliance

The BETA value is not critical as long as it keeps to the condition BETA >> KP. The pinch off voltage we have to vary in such a manner that we will reach the best fit of the resultant curve to the measurements. The maximum V_P value for one of the three JFET can be estimated from the V_{DS} voltage, at which the VDMOS attains the pinch off range (for the maximum gate voltage curve). For the other JFET we choose lower, nearly linear graduated V_P values.

2.4. Measurement and Simulation Results

This section outlines some simulation results of a MOS - JFET subcircuit according to Fig. 0C for case 2 in comparison to the measurements performed previously[9]. The simulation was made using the Level 3 model and the parameters shown in table 1 and 2 . Additional to the JFET effect we used the Level 3 - parameters THETA and VMAX to reduce the drain current. For VMAX we used the default value and THETA was found by fitting the transfer characteristic. The MOS transconductance, found for one transistor (756 µA V^{-2}), was divided evenly to the three devices. RS and RD are set to zero.
The parameters for the JFET's we chose according to case 2 described above. The BETA value is according to the condition BETA = 100 * KP and V_P varies from -5 to -22 V. The LAMBDA values we have determined by curve fitting.
The simulated results, shown in Fig. 1 to 3, are close in agreement with the experimental results.

KP / A V^{-2}	VTO / V	THETA / V^{-1}	VMAX / ms^{-1}
252 µ	1.85	158 m	5E4

Table 1: MOS model parameter

	JFET 1	JFET 2	JFET 3
VTO / V	- 5.3	- 9.7	- 22
BETA / A V^{-2}	25.2 m	25.2 m	25.2 m
LAMBDA	-15 m	- 18m	- 22 m

Table 2: JFET model parameter

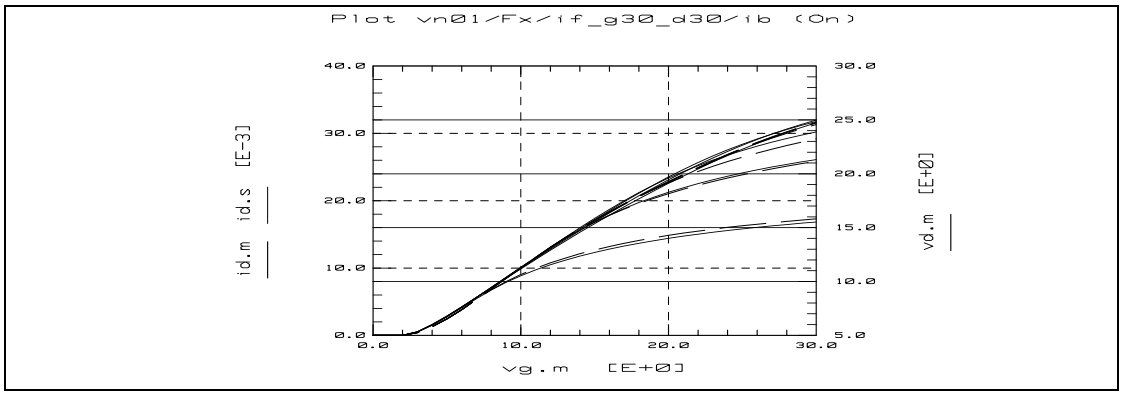

Fig. 1: Transfer Characteristic $I_D = f (V_{GS})$,V_{DS} = 5 ... 30 V, Step = 5 V

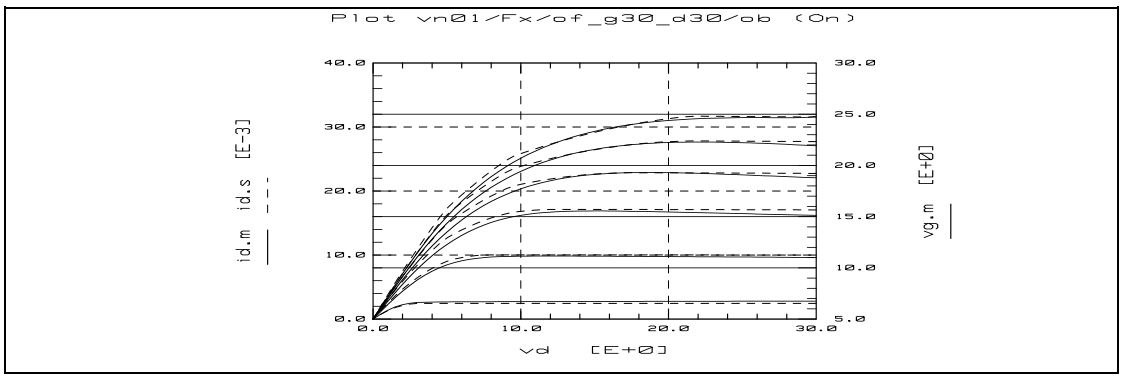

Fig. 2: Output Characteristic $I_D = f (V_{DS})$, V_{GS} = 5 ... 30 V, Step = 5 V and V_{DS} = 0 ... 30 V

[9] The DUT for all charcteristics is the one cell VDMOS transistor VN01(SMI - MIX2 - technology).

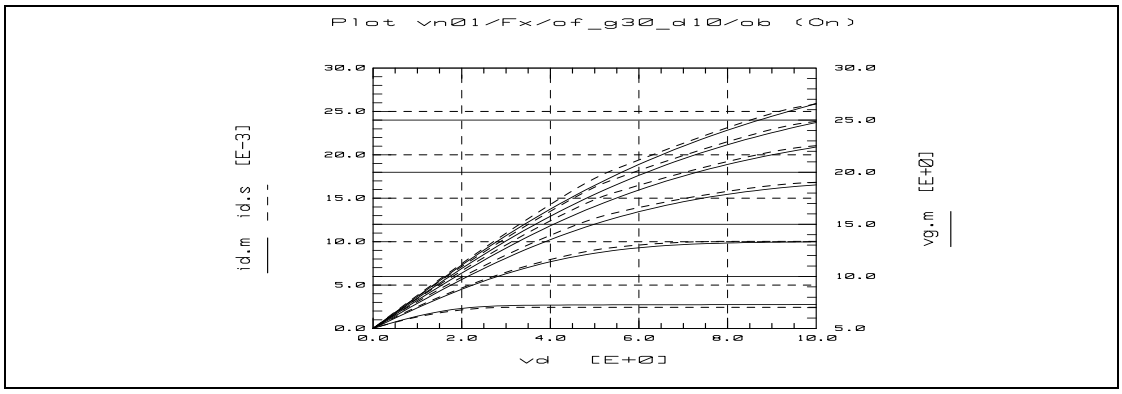

Fig. 3: Output Characteristic $I_D = f (V_{DS})$,V_{GS} = 5 ... 30 V, Step = 5 V and V_{DS} = 0 ... 10 V

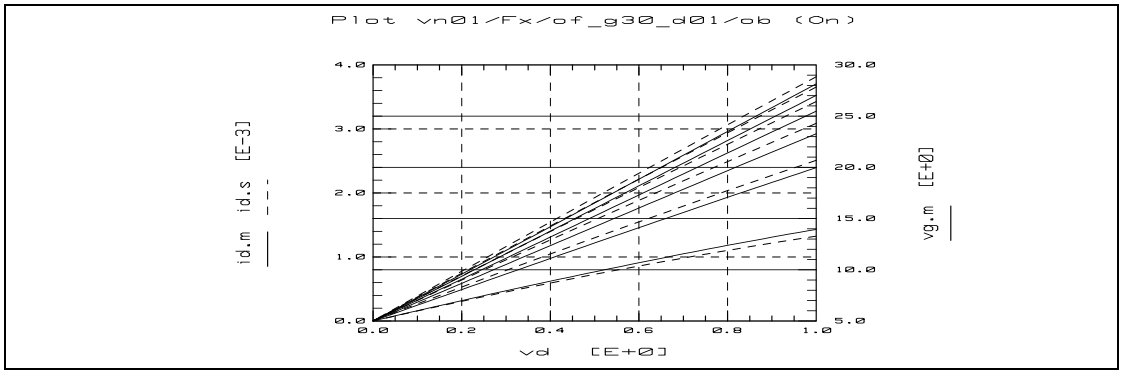

Fig. 4: Output Characteristic $I_D = f (V_{DS})$, V_{GS} = 5 ... 30 V, Step = 5 V and V_{DS} = 0 ... 1 V

3. Subcircuit Model using Voltage Controlled Voltage Source

3.1. Subcircuit Function

This section outlines the reduction of the effective gate voltage, using a transformation by a voltage controlled voltage source (VCVS). We used a polynomial VCVS (type E, see Fig. 5). For higher external gate voltages the MOS receives a reduced inner gate voltage. Thus the simulated drain current is reduced also. Polynomials of third or fourth order are suitable without absolute term:

$$V_{gs} = d * [V_{GS}]^4 + c * [V_{GS}]^3 + b * [V_{GS}]^2 + a * V_{GS} \qquad (2)$$

In reality we have completed the subcircuit by an additional MOS transistor M2 (Fig. 5B), receiving the full external gate voltage. In the case of low injection this device carries nearly 10 % of the drain current and is used to model the decrease in the output characteristic for high gate and drain voltages. The MOS devices are simulated by the Level 2 model. This allows the use of negative LAMBDA values for this purpose again.

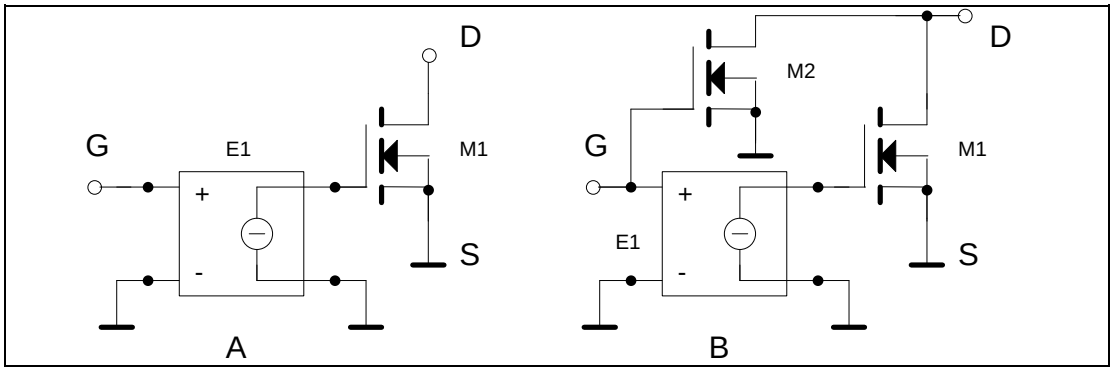

Fig. 5: Subcircuit using a VCVS, principle (A) and improved circuit (B)

3.2. Model Parameter Determination

Assuming the MOS parameters V_{TH} , K_P and R_S are known according to the methods described above now it is necessary to determine the polynomial coefficients. In a first step we have to determine the value of the reduced gate voltage V_{gs} for each output characteristic curve. This was simple made by fitting the simulated line to the measured line. The gate voltage, used for the simulation, was reduced until simulation and measurement are in agreement. This procedure was repeated for each external gate voltage step and we get a number of V_{gs} values (Table 3). Using an appropriate mathematical program we are able to determine the coefficients for the polynomial (Table 4).

V_{GS}	0	4	5	10	15	20	25	30
V_{gs}	0	4	4.85	7.8	9.8	11	12	12.4

Table 3: Values for the reduced gate voltage

a	b	c	d
1.209	- 0.056	0.0015	- 1.78 E-5

Table 4: Polynomial coefficients

3.3. Measurement and Simulation Results

The simulation was made using the circuit according to Fig. 5B, the coefficients from Table 4 and the model parameters for the MOS transistors in Table 5. The results are relatively close in agreement to the measurements.

	VTO / V	KP / A V^{-2}	RS / Ohm	RD / Ohm	LAMBDA
M1	1.85	680.4 µ	116.7	47.8	3.5 m
M2	1.85	75.6 µ	1050	430	-16 m

Table 5: Model parameter for MOS transistors [10]

[10] RD was determined at a relatively low gate voltage (VGS = 4 V).

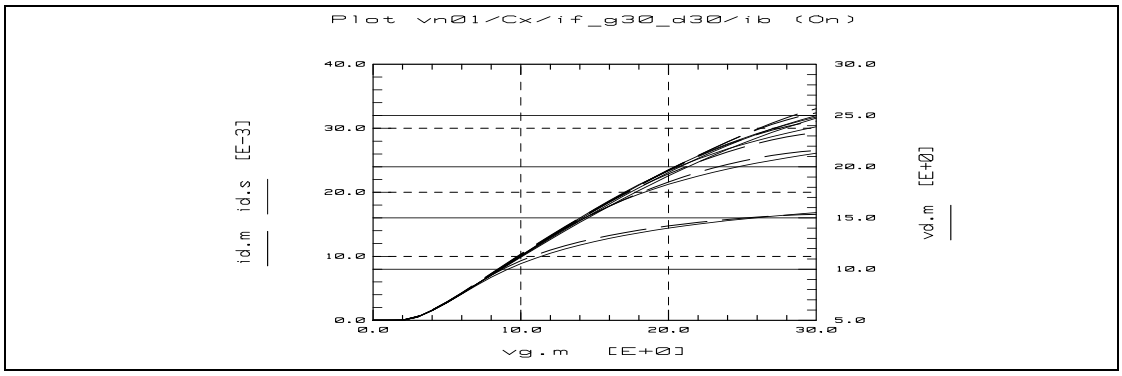

Fig. 6: Transfer Characteristic $I_D = f (V_{GS})$, V_{DS} = 5 ... 30 V, Step = 5 V, V_{GS} = 5 ... 30 V

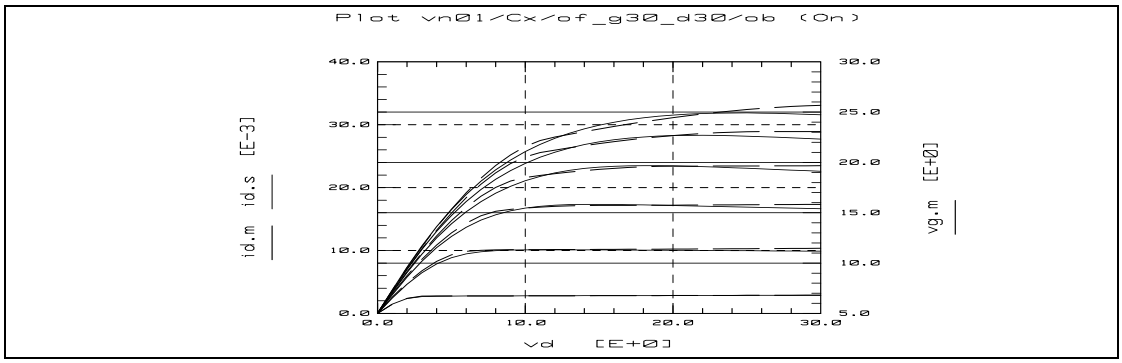

Fig. 7: Output characteristic $I_D = f (V_{DS})$, V_{GS} = 5 ... 30 V, Step = 5 V and V_{DS} = 0 ... 30 V

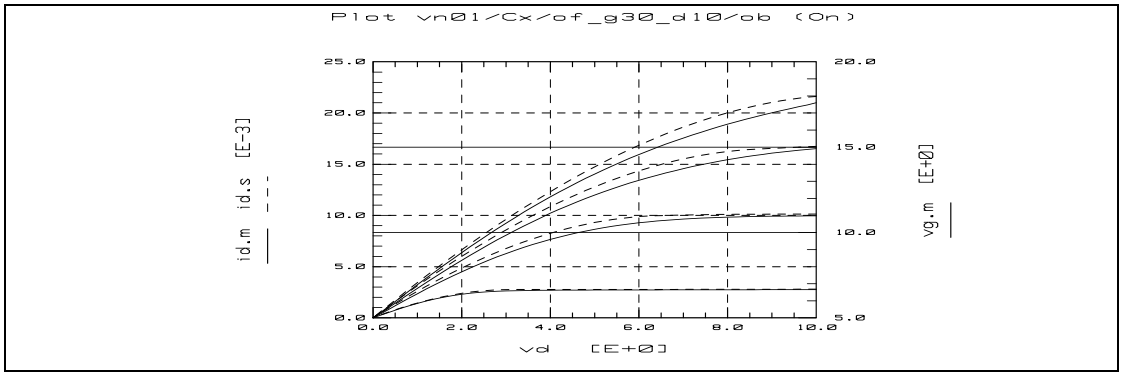

Fig. 8: Output characteristic $I_D = f (V_{DS})$, V_{GS} = 5 ... 30 V, Step = 5 V and V_{DS} = 0 ... 10 V

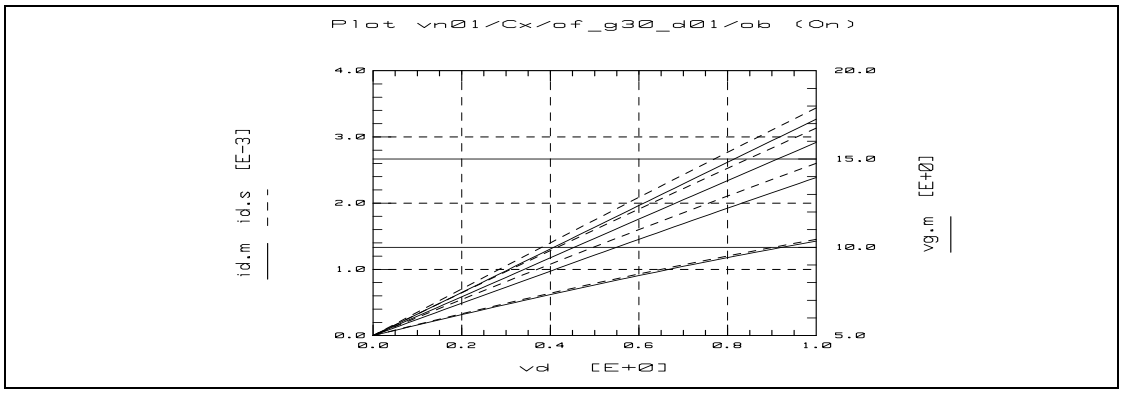

Fig. 9: Output characteristic $I_D = f (V_{DS})$, V_{GS} = 5 ... 30 V, Step = 5 V and V_{DS} = 0 ... 1 V

4. Conclusions

Two different methods for VDMOS subcircuit modeling have been analysed: a JFET - MOS subcircuit and a subcircuit using a VCVS. Methods for parameter extraction for both versions have been described.
The JFET version, using three branches, gives a good agreement to the measurements, but the parameter extraction is quite complicated.
The accuracy of the VCVS version results are comparable. The parameter extraction process is direct and is easy to use.
Both models take into account the self heating effect in a first order approximation.

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