Method for Determining the Effective Base Resistance of Bipolar Transistors

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ABSTRACT :

A simple DC method for integrated transistor base resistance extraction is described. Unlike other commonly-used DC methods, it doesn't need any knowledge about emitter or collector resistances. It is based on monitoring the substrate current of the parasitic vertical pnp transistor, when the intrinsic npn transistor is saturated.

1. Introduction

The base resistance is one of the most important modelling parameters for bipolar transistors. It is a non linear function of the base current. At low current values it is constant and its value is equal to one third the resistance of the base from one side of the emitter to the other [1]. At high current values the resistance drop can be attributed to two phenomena : the base conductivity modulation and the emitter current crowding; the latter tends to be the most important as the transistor geometry decreases. This behaviour is modelled by a set of three parameters, so that conventional network theory can be applied. The parameters are RB, the low-current maximum value, RBM, the minimum value at high current, and IRB, the current at which R_{bb} (the actual base resistance) is equal to (RB+RBM)/2. The physical dependence of these parameters on bias condition and process parameter is described by Hauser [2].

Several methods have been developed to extract the base resistance, which can be divided into three classes : noise measurements, DC measurements and high frequency AC measurements. Usual DC methods are quite simple to perform [3], but generally have poor accuracy and often require to precisely know the value of emitter resistance or need a special test structure [4]. High frequency methods are more versatile and better reflect the in-use base resistance [5,6,7] but they involve expensive material such as a network analyser and are quite long due to HF calibration.

A new, quick method of base resistance extraction is developed here, which uses the particular structure of integrated transistors for R_{bb} calculation and has the advantage of furnishing a value independent of other series resistances such as R_E or R_C.

2. Structure of an Integrated Bipolar Transistor

Figure 1 shows the usual cross-section structure of an integrated-circuit npn bipolar transistor, including the parasitic pnp. The resulting schematic is presented in figure 2.

In normal use, the base-collector junction is reverse biased ($V_{BC}<0$) and the substrate pin is tied to the lowest voltage, which means that the collector-substrate junction is reverse-biased, so the pnp is in off state and the substrate current is zero. But if the npn becomes saturated ($V_{BC}>0$) the pnp starts driving. Thus the base, collector and substrate of the npn transistor will behave as the emitter, base and collector of the pnp transistor, respectively, as shown in figure 2.

Figure 1 shows an interpretation of the base resistance. Generally speaking, it can be divided up to an external part, given by the resistance of the path from base contact to emitter edge, and an internal part, distributed on the base region below the emitter. The external part can be assumed as constant, whereas the internal part varies with base current, due to its distribution over the active area.

3. Description of the Method

The method described here uses the parasitic pnp to determine the base resistance; the equivalent circuit is assumed to be that of figure 2.

Basically, it consists in retrieving the V_{Rbb} voltage drop in the base resistance from currents and voltages measured on the B, E, C or S terminals; R_{bb} is then calculated by dividing by the base current I_B. This is the definition of the DC or large-signal base resistance of a BJT. The AC small-signal resistance can be calculated by [6]:

$$r_{bb} = R_{bb} + (dR_{bb} / dI_B)\, I_B \qquad (1)$$

For these measurements, all voltages applied to the transistor are referred to the base potential (B terminal); it means, V_B is set to 0V.

The emitter potential of the npn (E terminal) is such that the base-emitter junction is forward-biased (about -0.4V to -1V), making the npn ready to be on. The collector current is forced to zero, so that the voltage drop in R_C is zero; therefore, the measured collector voltage (V_C) is equal to the internal collector voltage, and influence of R_C is eliminated. In this case the npn is saturated, the base-collector junction is forward-biased and the pnp is ready to be on. The substrate is tied to a sufficiently negative value, so that the pnp works under linear conditions (not saturated).

Under these conditions, if the internal base-emitter voltage of the pnp is called V_{BEpnp}, the voltage drop in the base resistance is expressed by :

$$V_{Rbb} = V_{BEpnp} - V_C \qquad (2)$$

which permits to calculate the base resistance:

$$R_{bb} = V_{Rbb} / I_B = (V_{BEpnp} - V_C) / I_B \qquad (3)$$

Sweeping V_E from , for example, -0.4V to -1V, a variation of I_B is obtained and the curve of R_{bb} versus $\log(I_B)$ can be plotted. An extraction of the parameters RB, RBM and IRB can then be easily made from that curve. However, there is no mean to measure directly V_{BEpnp}.

3.1 Determination of the pnp Transistor Base-Emitter Voltage V_{BEpnp}

The pnp transistor base-emitter voltage V_{BEpnp} can be determined by inspecting the Gummel plot of the pnp transistor. The measurement setup for the Gummel plot is the same as the above mentioned. As shown in figure 3, the substrate current I_S deviates from the ideal substrate characteristics I_{S0} in the high-current region, due to the base resistance. High current injection does not occur in this case, because the base of the parasitic transistor is constituted of the collector area of the npn followed by the buried layer (figure 1), which is usually thick enough to consider it as the major part of the pnp base. Due to its heavy doping level, it is not concerned by high-current phenomena.

Based on that assumption, the relation between I_S and the internal V_{BEpnp} of the pnp simplifies to the ideal exponential law:

$$I_{S0} = I_{sat} \exp (V_{BEpnp} / (NF^*VT)) \qquad (4)$$

with $VT = kT / q$ is the thermal voltage, I_{sat} is the saturation current and NF is the emission coefficient.

From figure 3 the parameters I_{sat} and NF can be calculated by fitting the I_S-curve in the low bias region. With these values the ideal characteristic I_{S0} can be determined, which permits to identify the internal pnp base-emitter voltage V_{BEpnp}.

The low-current area in figure 3 is used to extract the idealised Gummel plot of the pnp as said above. With this result the internal pnp base-emitter voltage can be determined from the high-current area and R_{bb} can be extracted applying equation 3.

3.2 Accuracy of the Method

The accuracy of the R_{bb} calculation should be considered. The actual value of R_{bb} is obtained from measured V_C, I_B and extrapolated V_{BEpnp} as following:

$$R_{bb} = (V_{BEpnp} - V_C) / I_B \qquad (5)$$

leading to a relative error of the form:

$$\Delta R_{bb} / R_{bb} = (\Delta V_{BEpnp} + \Delta V_C) / (V_{BEpnp} - V_C) + \Delta I_B / I_B \quad (6)$$

Smaller the difference between V_C and V_{BEpnp} will be, greater becomes this relative error. As a result, the accuracy on R_{bb} will decrease for lower I_B values. To maintain an acceptably low error on R_{bb}, the accuracy of V_C and V_{BEpnp} should be as high as possible. For example, a base resistance which reaches its maximum value RB=300Ω at I_B=1mA will yield a voltage drop V_{Rbb}=300mV at this current. To estimate the R_{bb} value with correct accuracy, the error on V_{Rbb} should not exceed a few mV.

Since V_C is measured, its accuracy will be principally given by the measurement device resolution. Correct results can be obtained with an HP4155 set to a long integration time, which yields an accuracy of 2μV.

4. Measured Results

All measurements have been performed with an HP4155 semiconductor parameter analyser, and data analysis have been implemented using IC-CAP parameter extraction language [8].

The extraction method has been applied to several transistors of different technologies. Results have been compared to those obtained with the commonly-used AC input impedance circlefit method (figure 4) [5]. It should be noted that results agree quite well. The technology in this example is a standard 8GHz bipolar process.

Measurements have been performed with an external 27 Ω series resistance and compared with direct measurements. It appears that the difference correctly matches the external resistance for high currents but becomes more inaccurate as the current decreases (Figure 5). This is due to the fact, that at low current the effective base resistance value is much higher than the

additional series resistance value. For this example a 6GHz BiCMOS process was used.

Figure 6 compares measurements performed on transistors with identical emitter surface, but having one or two base contacts as illustrated on figure 7. It can be seen, that the results do not agree with the simplified theory, where a diminution of a factor 4 is expected. This is due to 2-D effects and agrees very well with the study performed by [9]. In this case measurements have been performed on devices issued from a 5GHz complementary technology.

Using devices from this process this method was applied with success on vertical pnp transistors.

Finally a SPICE parameter extraction and simulation was performed. The extracted parameters are RB, IRB and RBM. Figure 8 compares measurement and simulation; the agreement is very good in the medium and high current region.

5. Summary

A simple DC method for integrated transistor base resistance extraction was exposed. Unlike other commonly-used DC methods, it doesn't need any knowledge about emitter or collector resistances. It can be applied to both npn and vertical pnp devices. From the obtained $R_{bb}(I_B)$ characteristic the extraction of the model parameters is straightforward. Using these parameters a good agreement between measured and simulated device characteristics is achieved with the standard BJT model developed by Gummel and Poon.

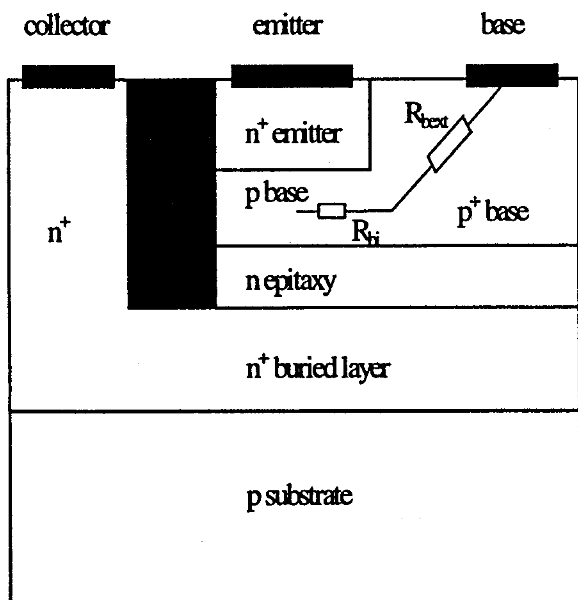

Fig 1: Device cross section of a integrated npn transistor

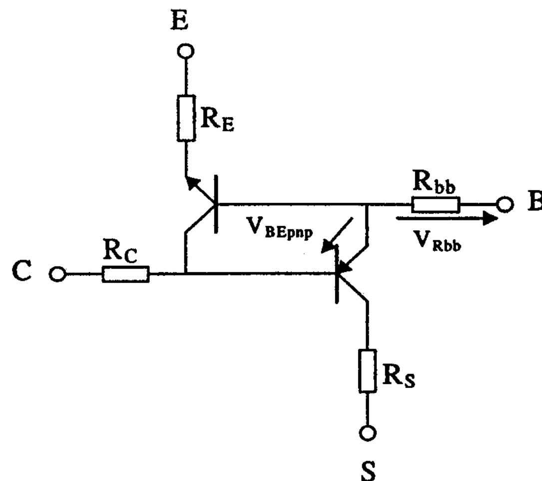

Fig 2 : Equivalent circuit including the parasitic pnp transistor

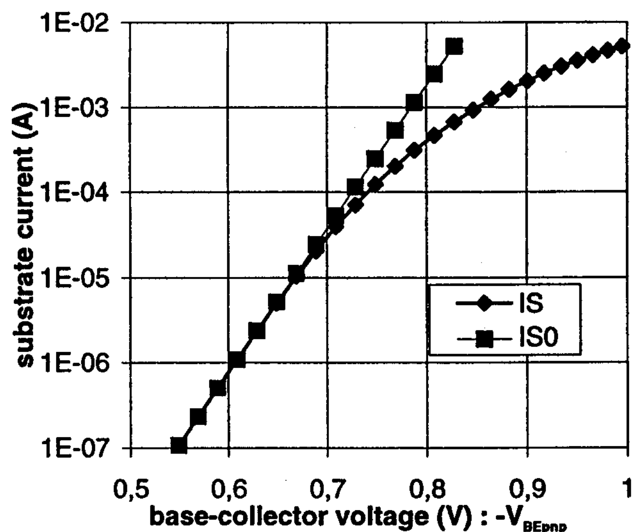

Fig 3 : idealised and real substrate current versus base-collector voltage

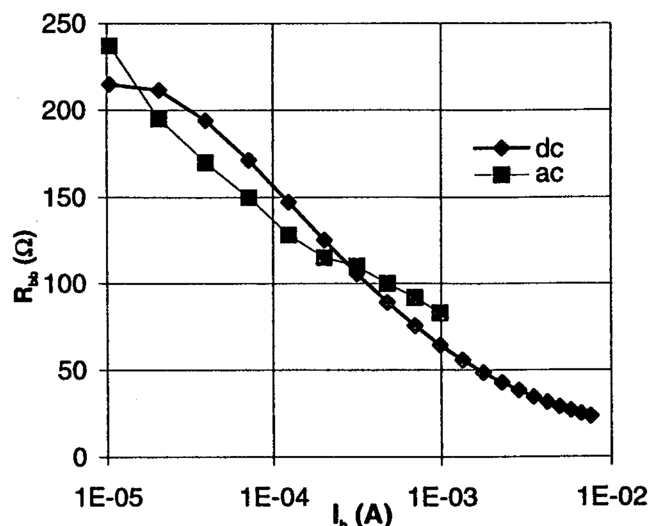

Fig 4 : Comparison of the R_{bb} resistance using the proposed DC method and the circle fit AC method

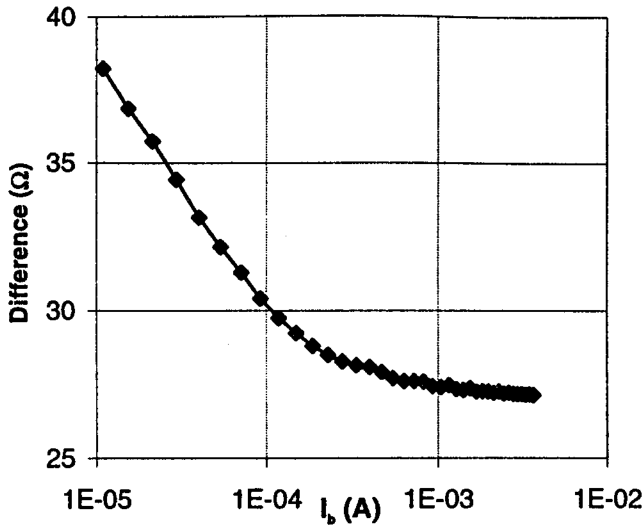

Fig 5: Difference of the $R_{bb}(I_B)$ determination with and without a additional series resistance of 27 Ω

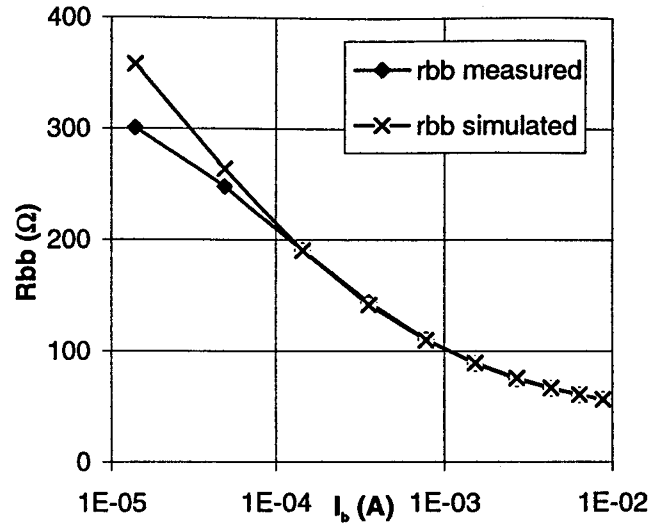

Fig 8 : Comparison of measured and simulated $R_{bb}(I_b)$ behaviour using the standard Gummel-Poon model

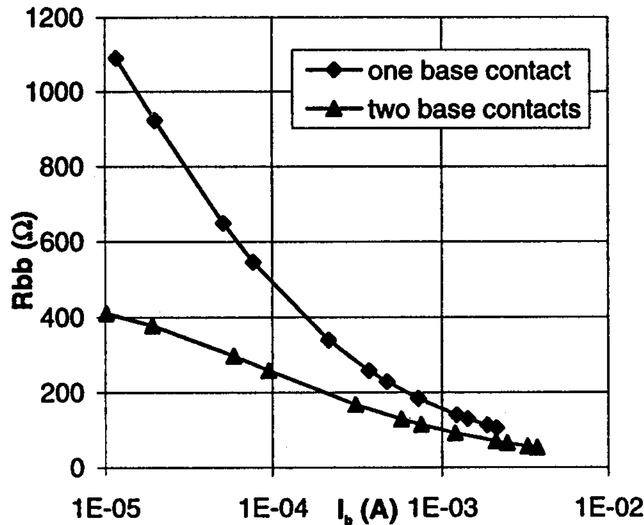

Fig 6 : $R_{bb}(I_B)$ determination for transistors with different geometries

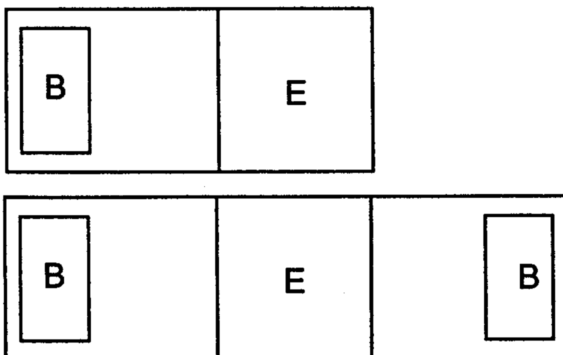

Fig 7 : single and doubled base contact structures, the emitter is walled

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