Emitter and Collector Resistance Determination for Integrated Lateral PNP Transistors using Substrate Effects[1]

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Abstract - This paper is concerned with the modeling of integrated lateral bipolar transistors. It's behaviour is affected by two parasitic devices, the vertical emitter device (VED) and the vertical collector device (VCD). Usually a subcircuit model is used, taking into account these parasitic transistors. This results in a better simulation of the DC - characteristics, including the substrate current, compared to the SGP - model.
Taking advantage of substrate effects, we found new methods for emitter and collector series resistance determination for the PNP lateral transistor subcircuit model.

1 Introduction

It is well known, that an integrated lateral transistor consists of the main lateral device (LD) and two parasitic devices:

- the parasitic emitter device (PED), consisting of emitter, epitaxy and substrate layer
- the parasitic collector device (PCD), consisting of collector , epitaxy and substrate layer

Fig 1 shows the appropriate subcircuit model. PED is active, whenever the main lateral device LD is in the active forward mode. Both the p - type collector and the p - type isolation (= substrate) act as a collector then. PCD however is only active, if LD is in saturation mode or in the inverse mode. During floating voltage measurements on several lateral transistor types [2] we observed, that the floating voltage at the collector terminal is affected by the substrate potential, and vice versa. There are four situations possible, referring to the bias at the collector and the substrate terminal:

- A) collector terminal and substrate terminal negative biased
- B) collector terminal floating, substrate terminal negative biased
- C) collector terminal negative biased, substrate terminal floating
- D) collector terminal and substrate terminal floating

These situations give rise to determine the vertical emitter resistance R_{EV} , the lateral emitter resistance R_{EL} and the collector resistance R_C .

[1] This paper is intended for the HP User Meeting Oct. 1997 Berlin, Rev.:14.6.97, 10.9.97

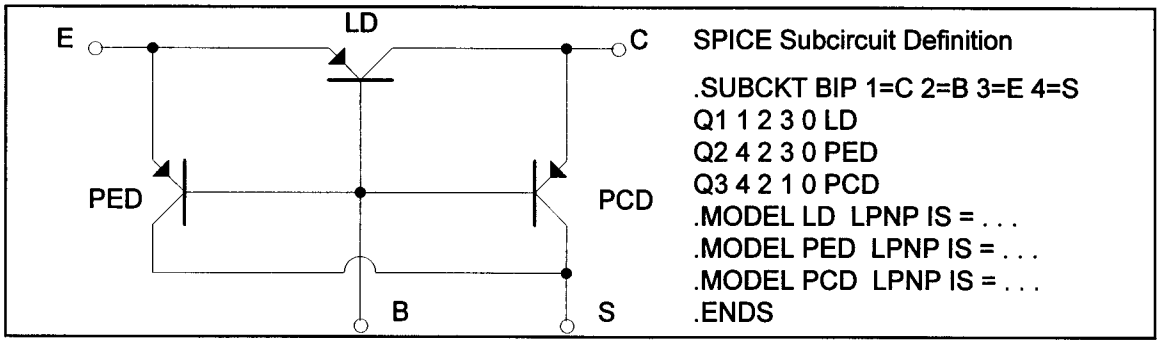

Fig 1: Subcircuit model of an integrated PNP - lateral transistor

2 Emitter Resistance Determination

This section describes a method for the emitter series resistance determination for both the main lateral device (LD) and parasitic emitter device (PED).

2.1 Vertical Emitter Resistance R_{EV}

The method for R_{EV} determination is based on the following observation: the floating voltage at the collector terminal V_{CF} depends on the substrate potential. If the substrate is floating too, V_{CF} is low. However, if the substrate potential is defined using a negative voltage V_S , the floating voltage V_{CF} rises.

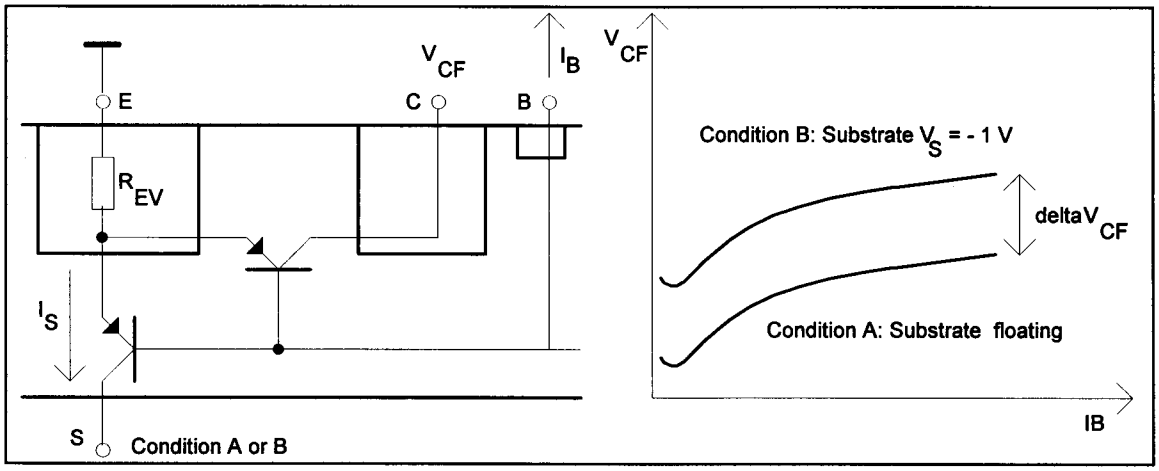

Fig 2: Collector - floating voltage V_{CF} for floating substrate condition (A) and negative substrate voltage condition (B)

As can be seen from Fig 2, this voltage shift is created by the vertical transfer current of the PED, working in the active forward mode at negative substrate potential condition. This vertical current creates in the emitter region a voltage drop at the vertical emitter resistance. Consequently the collector floating voltage is shifted by the same amount. We are able to calculate a resistance using the voltage shift and the appropriate substrate current, interpreting this resistance as the vertical component of the emitter resistance:

$$R_{EV} = \frac{\Delta V_{CF}}{I_{Sub}} \qquad (1)$$

In this way a characteristics as given in Fig 3 were obtained. For high currents the R_{EV} - characteristic approaches a nearly constant value: For PP12 we get R_{EV} = 12 Ohm.

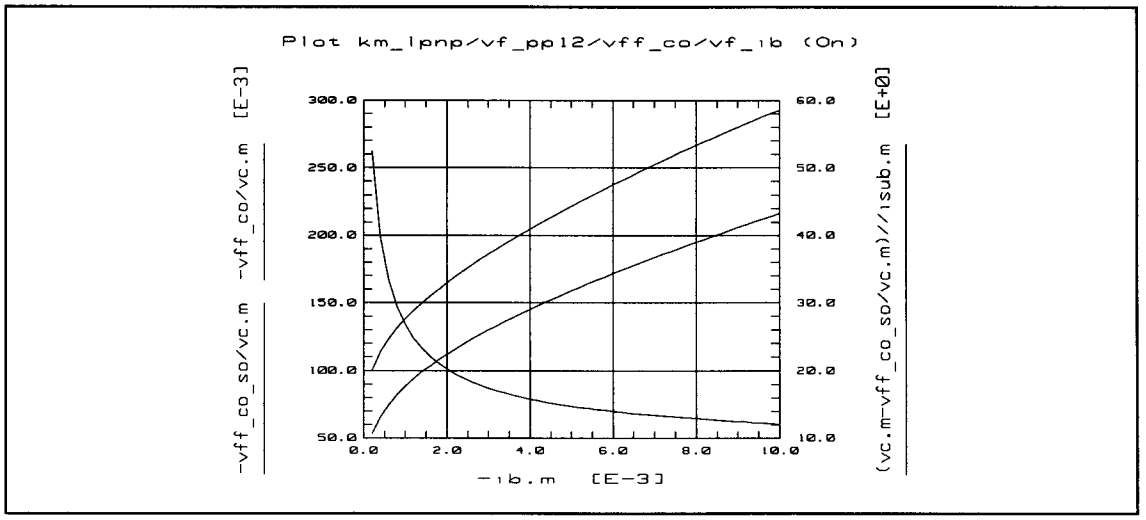

Fig 3: Collector - floating voltage V_{CF} and vertical emitter resistance for transistor PP12

2.2 Lateral Emitter Resistance R_{EL}

Similarly to the R_{EV} - determination we are able to find out the lateral component R_{EL} of the emitter series resistance: The floating voltage at the substrate terminal V_{SF} depends on the collector potential. If the collector is floating too, V_{SF} is low. However, if the collector potential is defined using a negative voltage V_C , the floating voltage rises.

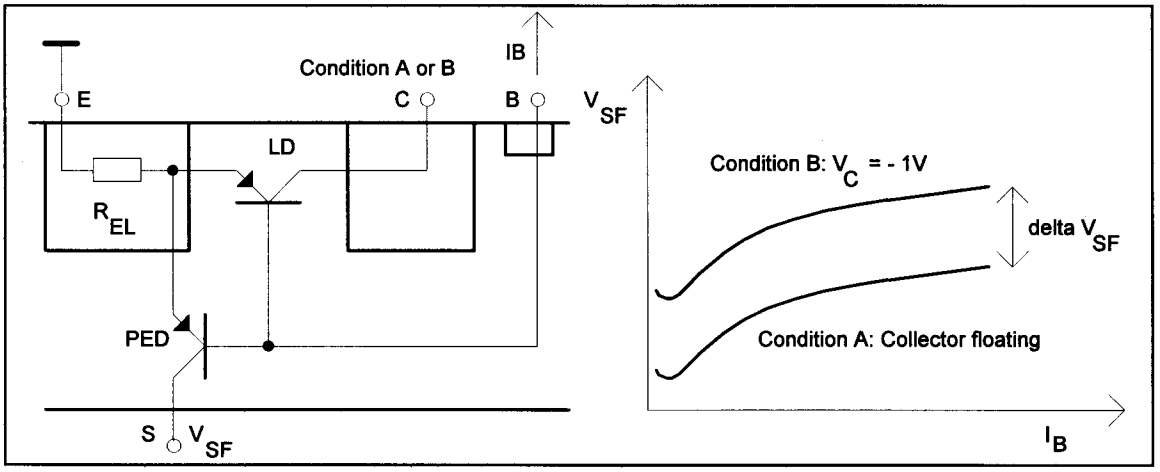

Fig 4: Substrate - floating voltage V_{SF} for floating collector condition (A) and negative collector voltage condition (B)

This voltage shift is created by the lateral transfer current of the LD, working in the active forward mode at negative collector potential condition. This lateral current creates in the emitter region a voltage drop at the lateral emitter resistance. Consequently the substrate floating voltage is shifted by the same amount. Using this voltage shift ΔV_{SF} the lateral emitter resistance component is given by:

$$R_{EL} = \frac{\Delta V_{SF}}{I_C} \qquad (2)$$

Again, we have a characteristic, striving to constant value at high currents. For PP12 we get R_{EL} = 20 Ohm.

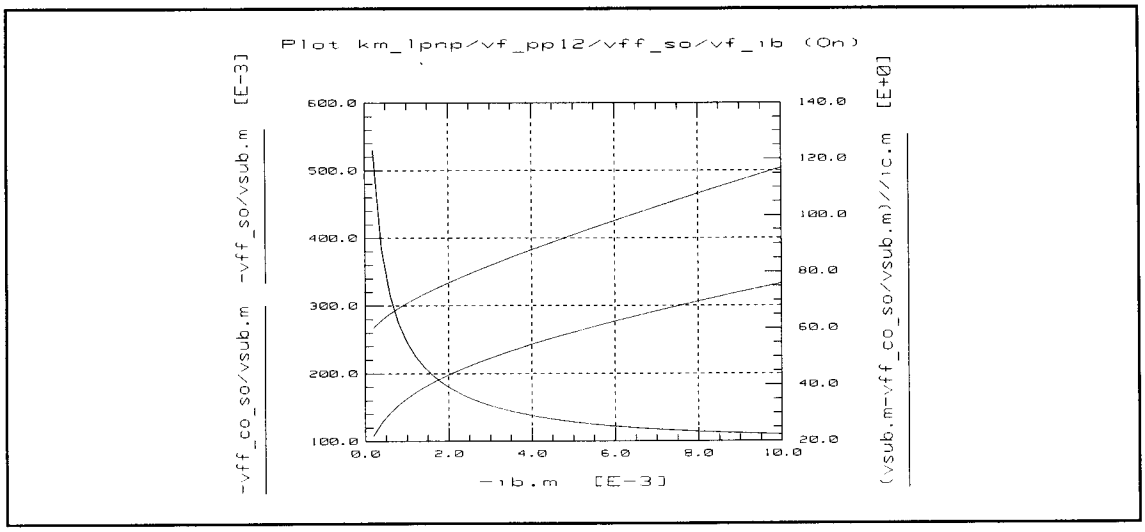

Fig 5: Substrate - floating voltage V_{SF} and lateral emitter resistance for transistor PP12

3 Collector Resistance Determination

The ΔI_{Sub} - method, described for npn - transistors in [3], is useful for lateral transistors too. This method is based on a modified Gummel plot measurement, using a slightly forward biased base - collector junction instead of $V_{BC} = 0$.

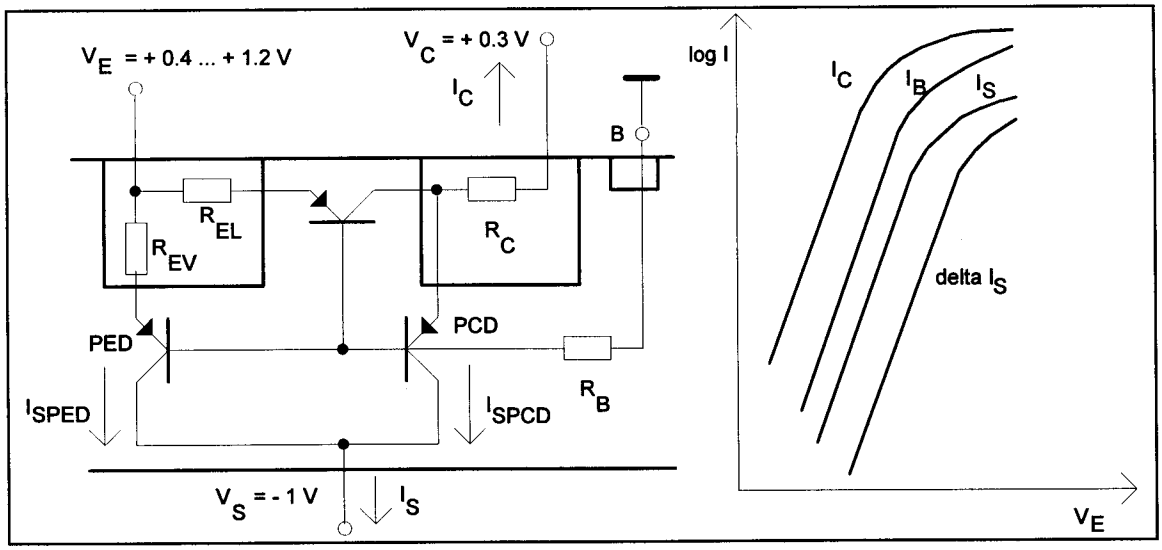

Fig 6: ΔI_{Sub} - method for the integrated lateral transistor

Fig 6 shows the conditions during this measurement. The substrate current I_S consists of two parts, the current I_{SPED} , created by the PED, and the current I_{SPCD} , created by the PCD. Considering an increasing voltage V_{BE} we observe:

- at low V_{BE} : The positive potential at the collector terminal causes the BC junction slightly forward biased. The substrate current I_S , showing a small and constant value, consists only of the current I_{SPCD}. , because I_{SPED} is negligible.
- at increasing V_{BE} : Both the PED and the LD are forward biased. The current I_{SPED} and the collector current I_C increase. Therefore, the collector resistance voltage drop, the base - emitter voltage of the PCD and the current I_{SPCD} increase too. The substrate current I_S consists of I_{SPED} and I_{SPCD} now.

Using the change of the substrate current I_{SPCD} , we are able to determine the collector resistance. Considering two points P1 and P2 we have for the collector voltage:

$$V_C = V_{RC1} + V_{EB(PCD)1} + V_{RB1} \tag{3}$$

and

$$V_C = V_{RC2} + V_{EB(PCD)2} + V_{RB2} \tag{4}$$

The collector resistance is given by:

$$R_C = \frac{\Delta V_{EB(PCD)} - \Delta V_{RB}}{I_{C1} - I_{C2}} \tag{5}$$

We can determine $\Delta V_{EB(PCD)}$ using the substrate current values I_{SPCD} (P1) and I_{SPCD} (P2):

$$\Delta V_{EB(PCD)} = V_T \ln \frac{I_{SPCD}(P2)}{I_{SPCD}(P1)} \tag{6}$$

Assuming a constant base resistance voltage drop ($V_{RB1} \approx V_{RB2}$)[2] and combining eqn (5) and (6) we have for R_C :

$$R_C = \frac{V_T \ln \frac{I_{SPCD}(P2)}{I_{SPCD}(P1)}}{I_{C1} - I_{C2}} \tag{7}$$

There is a problem using eqn (7): we are not able to measure I_{SPCD} directly. Consequently we have to use a two step method:

- Step 1: Gummel plot measurement for V_{BC} = 0, e.g. the transistor acts in the active forward mode. The substrate current consists only of I_{SPED} in this case.
- Step 2: Gummel plot measurement for negative V_{BC} as described above. I_S consists both of I_{SPED} and I_{SPCD} now.

The substrate current part I_{SPCD} can be calculated now as:

$$I_{SPCD} = I_S(STEP2) - I_S(STEP1) \tag{8}$$

Using this method for transistor PP12 we found a collector resistance of 112 Ohm[3].

	P1	P2
V_E / mV	750	800
I_{SPCD} / nA	14,4	75
I_C / µA	273	641
I_B / µA	37	163

Table 1: Measurement values for RC calculation

[2] This is given at a sufficient high base current, where R_B is nearly constant. The determination of $R_B(I_B)$ using the circle fit method [4] is useful to check this condition.

[3] Taking into account the base resistance of 40 ... 20 Ohm for I_B = 30 ... 100 µA the calculated value reduces to R_C = 93 Ohm.

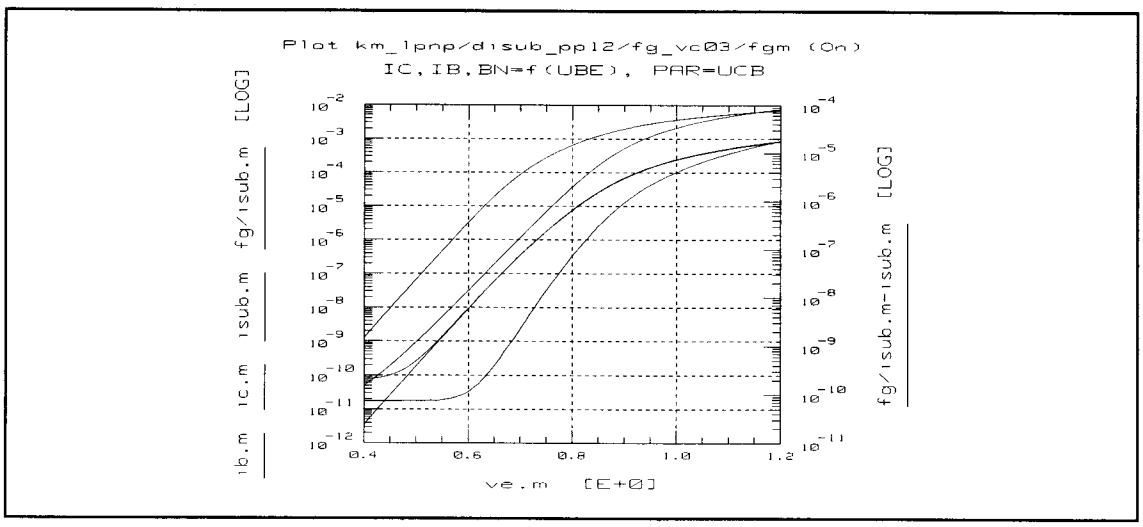

Fig. 7: RC - determination using the ΔI_{Sub} - method for transistor PP12, V_C = + 0.3 V

4 Summary

An integrated lateral transistor consist of the main lateral and two parasitic devices, PED and PCD. Taking into account the effects of the parasitic devices on the substrate current respectively substrate voltage we are able to determine the emitter and the collector series resistances:

- The change in the substrate floating voltage referring to the collector potential gives rise to determine the lateral emitter resistance
- The change in the collector floating voltage referring to the substrate potential gives rise to determine the vertical emitter resistance
- The change in the PCD substrate current gives rise to determine the collector resistance.

5 References

[1] Kulke, B., Miller, S.L.: "Accurate Measurements of Emitter and Collector Series Resistances in Transistors". Proc. IRE Vol. 45, 1957, pp. 90

[2] Berkner, J. : "Bahnwiderstandsmessungen zum AI1017". HFO, Labornotiz vom 18.4.91

[3] Berkner, J.: "A Survey of DC - Methods for Determining the Series Resistances of Bipolar Transistors including the new Δ ISub - Method". In: 1st Combined European Hewlett Packard HP4062 & IC-CAP User Meeting Proceedings, 9. -12.10.94, Hourburg Wihr

[4] Sansen,W.M.C., Meyer, R.G: "Characterization and Measurement of the Base and Emitter Resistance of Bipolar Transistors". IEEE Journal of Solid State Circuits, No.6, Dec.72, pp.492 - 498